



Substitute for Form 1449A/PTO  
**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
(Use as many sheets as necessary)

Complete if Known

<b>Application Number</b>	10/763136
<b>Filing Date</b>	January 22, 2004
<b>First Named Inventor</b>	Forbes, Leonard
<b>Group Art Unit</b>	Unknown
<b>Examiner Name</b>	Nguyen, Tuan

Sheet 1 of 4

Attorney Docket No: 303.588US3

**US PATENT DOCUMENTS**

Examiner Initials*	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
<i>Dr</i>	US-2003/0235075 A1	12/25/2003	Forbes, L.	365	177	06/21/2002
	US-2003/0235077 A1	12/25/2003	Forbes, L.	365	185.05	06/21/2002
	US-2003/0235081 A1	12/25/2003	Forbes, L.	365	185.28	06/21/2002
	US-2003/0235085 A1	12/25/2003	Forbes, L.	365	189.09	06/21/2002
	US-3,805,130	04/16/1974	Yamazaki, S.	317	235B	07/03/1973
	US-4,173,766	11/06/1979	Hayes, James A.	357	23	09/16/1977
	US-4,661,833	04/01/1987	Mizutani, Yoshihisa	365	185.01	10/29/1985
	US-4,939,559	07/03/1990	DiMaria, , et al.	357	23.5	04/01/1986
	US-5,298,447	03/29/1994	Hong, G.	437	43	07/22/1993
	US-5,493,141	02/20/1996	Ricco, B. , et al.	257	321	04/21/1994
	US-5,740,104	04/14/1998	Forbes, Leonard	365	185.03	01/29/1997
	US-5,768,192	06/16/1998	Eitan, Boaz	365	185.24	07/23/1996
	US-5,781,477	07/14/1998	Rinerson, Darrell D., et al.	365	185.29	02/23/1996
	US-5,959,896	09/28/1999	Forbes, L.	365	185.33	02/27/1998
	US-6,038,168	03/14/2000	Allen, A. J., et al.	365	185.07	06/26/1998
	US-6,191,445	02/20/2001	Fujiwara, I.	257	321	11/04/1998
	US-6,229,733	05/08/2001	Male, B.	365	185.18	12/30/1999
	US-6,469,352	10/22/2002	Ohshima, K. , et al.	257	355	06/20/2001
	US-6,521,958	02/18/2003	Forbes, L. , et al.	257	391	08/26/1999
	US-6,577,263	06/10/2003	Saito, Y.	341	155	10/30/2002
	US-6,614,693	09/02/2003	Lee, J. , et al.	365	185.29	03/19/2002
<i>Dr</i>	US-6,700,821	03/02/2004	Forbes, L. , et al.	365	189.01	08/08/2001

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
--------------------	---------------------	------------------	---	-------	----------	----------------

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No'	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
<i>Dr</i>		"MT28F002B5 Flash Memory Data Sheet", Micron Technology, Inc., (Jan	

EXAMINER

*Tuan T. Nguyen*

DATE CONSIDERED

*9/17/04*

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>		<i>Complete if Known</i>	
		<b>Application Number</b>	10/763136
		<b>Filing Date</b>	January 22, 2004
		<b>First Named Inventor</b>	Forbes, Leonard
		<b>Group Art Unit</b>	Unknown
		<b>Examiner Name</b>	Nguyen, Tuan
		Attorney Docket No: 303.588US3	

Sheet 2 of 4

### OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
<i>Du</i>		2000),	
<i>Du</i>		ADLER, E. , et al., "The Evolution of IBM CMOS DRAM Technology", <u>IBM Journal of Research &amp; Development</u> , 39(1-2), (January-March 1995),167-188	
		DEKEERSMAECKER, R. , et al., "Electron Trapping and Detrapping Characteristics of Arsenic-Implanted SiO(2) Layers", <u>J. Appl. Phys.</u> , 51, (Feb. 1980),1085-1101	
		DIMARIA, D. , et al., "Capture and Emission of Electrons at 2.4-eV-Deep Trap Level in SiO(2) Films", <u>Physical Review B</u> , 11, (June 1975),5023-5030	
		DIMARIA, D. , et al., "Enhanced Conduction and Minimized Charge Trapping in Electrically Alterable Read-Only Memories Using Off-Stoichiometric Silicon Dioxide Films", <u>J. Appl. Phys.</u> , 55, (April 1984),3000-3019	
		EITAN, BOAZ , "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell", <u>IEEE Electron Device Letters</u> , 21(11), (November 2000),543-545	
		FISCHETTI, M. V., et al., "The effect of gate metal and SiO <sub>2</sub> thickness on the generation of donor states at the Si-SiO <sub>2</sub> interface", <u>Journal of Applied Physics</u> , vol. 57, no. 2, (January 1985),418-424	
		FORBES, L. , et al., "Thermal Re-Emission of Trapped Hot Electrons in NMOS Transistors", <u>IEEE Trans. on Electron Devices</u> , 38, (Dec. 1991),2712	
		HANAFI, H. , et al., "Fast and Long Retention-Time Nano-Crystal Memory", <u>IEEE Trans. on Electron Devices</u> , 43, (Sept. 1996),1553-1558	
		HORI, T. , et al., "A MOSFET with Si-Implanted Gate-SiO(2) Insulator for Nonvolatile Memory Applications", <u>Int'l Electron Devices Meeting: Technical Digest</u> , San Francisco, CA,(Dec. 1992),469-472	
		HSU, C. , et al., "Observation of Threshold Oxide Electric Field for Trap Generation in Oxide Films on Silicon", <u>J. Appl. Phys.</u> , 63, (June 1988),5882-5884	
		HUNTLEY, D. , et al., "Deep Traps in Quartz and Their Use for Optical Dating", <u>Canadian J. Physics</u> , 74, (March/April 1996),81-91	
		HWANG, N. , et al., "Tunneling and Thermal Emission of Electrons at Room Temperature and Above from a Distribution of Deep Traps in SiO <sub>2</sub> ", <u>Proc. Int'l Elec. Devices and Materials Symp.</u> , Taiwan,(Nov. 1992),559-562	
		KALNITSKY, A. , et al., "Memory Effect and Enhanced Conductivity in Si-Implanted Thermally Grown SiO(2)", <u>IEEE Trans. on Electron Devices</u> , ED-34, (Nov. 1987),2372	
		KALNITSKY, A. , et al., "Rechargeable E' Centers in Silicon-Implanted SiO(2) Films", <u>J. Appl Phys.</u> , 67, (June 1990),7359-7367	
		LEE, M. , et al., "Thermal Self-Limiting Effects in the Long-Term AC Stress on N-Channel LDD MOSFET's", <u>Proc.: 9th Biennial University/Government/Industry Microelectronics Symp.</u> , Melbourne, FL,(June, 1991),93-97	
<i>Du</i>		LUSKY, ELI , et al., "Spatial characterization of Channel hot electron injection Utilizing subthreshold slope of NROM memory device", pp. 1-2	
		MILLER, A. , "Silicon Dioxide", MIT, <a href="http://www.ai.mit.edu/people/tkts/silicon-">www.ai.mit.edu/people/tkts/silicon-</a>	

EXAMINER

*Tuan T. Nguyen*

DATE CONSIDERED

*7/7/04*

(Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>		Complete if Known	
		<b>Application Number</b>	10/763136
		<b>Filing Date</b>	January 22, 2004
		<b>First Named Inventor</b>	Forbes, Leonard
		<b>Group Art Unit</b>	Unknown
		<b>Examiner Name</b>	Nguyen, Tuan
Sheet 3 of 4		Attorney Docket No: 303.588US3	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		dioxide.html,	
<i>Du</i>		NING, T. H., "Capture cross section and trap concentration of holes in silicon dioxide", <u>Journal of Applied Physics</u> , vol. 47, no. 3, (March 1976), 1079-1081	
		NING, T. H., et al., "Completely electrically reprogrammable nonvolatile memory device using conventional p-channel MOSFET", <u>IBM Technical Disclosure Bulletin</u> , vol. 20, no. 5, (October 1977), 2016	
		NING, T. H., et al., "Erasable nonvolatile memory device using hole trapping in SiO <sub>2</sub> ", <u>IBM Technical Disclosure Bulletin</u> , vol. 18, no. 8, (January 1976), 2740-2742	
		ROIZIN, YAKOV, et al., "'Dummy' GOX for Optimization of microFLASH Technology", 2 pages	
		ROIZIN, YAKOV, et al., "Activation Energy of Traps in the ONO Stack of microFLASH Memory Cells", 2 pages	
		SAMANTA, PIYAS, et al., "Coupled charge trapping dynamics in thin SiO <sub>2</sub> gate oxide under Fowler-Nordheim stress at low electron fluence", <u>Journal of Applied Physics</u> , vol. 83, no. 5, (March 1998), 2662-2669	
		TAKEUCHI, K., et al., "A Double-Level-V Select Gate Array Architecture for Multilevel NANAD Flash Memories", <u>IEEE Journal of Solid-State Circuits</u> , 31, (April 1996), 602-609	
		THOMAS, J. H., et al., "Electron Trapping Levels in Silicon Dioxide Thermally Grown on Silicon", <u>J. Physics and Chemistry of Solids</u> , Vol. 33, (1972), 2197-2216	
		THOMPSON, S., et al., "Positive Charge Generation in SiO <sub>2</sub> by Electron-Impact Emission of Trapped Electrons", <u>J. Appl. Phys.</u> , 72, (Nov. 1992), 4683-4695	
		THOMPSON, S., et al., "Tunneling and Thermal Emission of Electrons from a Distribution of Shallow Traps in SiO <sub>2</sub> ", <u>Appl. Phys. Lett.</u> , 58, (March 1991), 1262-1264	
		TIWARI, SANDIP, "Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage", <u>Int'l Electron Devices Meeting: Technical Digest</u> , Washington, DC, (Dec. 1995), 521-524	
		TYSON, J., "How Flash Memory Works", <u>www.howstuffworks.com/flash-memory.htm</u> , (1998-2000)	
		VUILLAUME, D., et al., "Charging and Discharging Properties of Electron Traps Created by Hot-Carrier Injections in Gate Oxide of N-Channel Metal Oxide Semiconductor Field Effect Transistor", <u>J. Appl. Phys.</u> , 73, (March 1993), 2559-2563	
		WOLF, S., "Ion Implantation for VLSI", <u>Silicon Processing for the VLSI Era</u> , Vol. 1, (1990), 280	
<i>Du</i>		WOLF, S., "MOS devices and NMOS process integration", In: <u>Silicon Processing for the VLSI Era</u> , Vol. 2, Lattice Press, Sunset Beach, CA, (1990), p.	

EXAMINER Tuan T. Nguyen DATE CONSIDERED 9/7/04

Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>		<i>Complete if Known</i>	
		<b>Application Number</b>	10/763136
		<b>Filing Date</b>	January 22, 2004
		<b>First Named Inventor</b>	Forbes, Leonard
		<b>Group Art Unit</b>	Unknown
		<b>Examiner Name</b>	Nguyen, Tuan
Sheet 4 of 4		Attorney Docket No: 303.588US3	

<b>OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
<i>Da</i>	319	WOLF, S. , "Thermal oxidation of single crystal oxidation", In: <i>Silicon Processing for the VLSI Era</i> , Vol. 1, Lattice Press, Sunset Beach, CA,(1990),p. 227	
<i>Da</i>		YOUNG, D. , et al., "Characterization of Electron Traps in Aluminum-Implanted SiO(2)", <i>IBM J. Research and Development</i> , 22, (May 1978),285-288	

EXAMINER

*Tuan T. Nguyen*

DATE CONSIDERED

*9/7/04*

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 606. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional); <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached